IN THE CLAIMS

Please amend the claims as follows:

1-44. (canceled)

45. (previously presented) A microprocessor system, comprising:
a microprocessing unit (MPU);
an input-output processor (IOP);
a global memory unit coupled to said MPU and to said IOP;
a direct memory access controller (DMAC);
an interrupt controller (INTC);
a programmable memory interface (MIF);
a CMOS oscillator, operating in conjunction with a clock multiplier;
a plurality of bit inputs; and
a plurality of bit outputs.

46. (previously presented) The microprocessor system of claim 45, wherein:
a frequency of said oscillator is doubled internally to operate said MPU and said IOP.

47. (previously presented) The microprocessor system of claim 45, wherein:
said microprocessor system utilizes a phase locked loop circuit.

48. (previously presented) The microprocessor system of claim 45, wherein:
said MPU retrieves up to four instructions from memory for each instruction fetch or pre-fetch.

49. (previously presented) The microprocessor system of claim 45, wherein:
said MPU fetches multiple sequential instructions from said global memory unit in parallel, and said global memory unit supplies said multiple sequential instructions to said MPU during a single memory cycle.

50. (previously presented) The microprocessor system of claim 45, wherein:
said MPU further comprises an arithmetic logic unit (ALU) that is used for data operations and for branch address calculations.

51. (previously presented) The microprocessor system of claim 45, wherein:
said MPU further comprises an arithmetic logic unit (ALU), and a first push down stack with a top item register and a next item register, connected to provide inputs to said ALU, an output of said ALU being connected to said top item register.

52. (previously presented) The microprocessor system of claim 45, wherein:
said MPU comprises a zero-operand dual-stack architecture.

53. (previously presented) The microprocessor system of claim 52, wherein:
said dual-stack architecture is cached on chip and automatically spills to and refills from external memory.

54. (previously presented) The microprocessor system of claim 45, wherein:
said MPU comprises a plurality of global data registers and a plurality of local registers.

55. (previously presented) The microprocessor system of claim 45, wherein:
said global memory unit is shared by said MPU, said IOP, and said MIF.

56. (previously presented) The microprocessor system of claim 45, wherein:
said global memory unit is used for data storage and control communication with said DMAC and said IOP.

57. (previously presented) The microprocessor system of claim 45, wherein:
said global memory unit is used by said IOP for transfer information, loop counts, and delay counts.

58. (previously presented) The microprocessor system of claim 45, wherein:
said MIF is shared by said IOP, said MPU, said DMAC, said plurality of bit outputs, and said plurality of bit inputs.

59. (previously presented) The microprocessor system of claim 45, wherein:
bus transaction requests are arbitrated and prioritized by said MIF.

60. (previously presented) The microprocessor system of claim 45, wherein:
said INTC is shared by said plurality of bit inputs, said IOP, and said DMAC.

61. (previously presented) The microprocessor system of claim 45, wherein:
said global memory unit comprises a plurality of global registers.

62. (previously presented) The microprocessor system of claim 61, wherein:
said plurality of global registers are used for operand storage for said MPU, and for data storage for said IOP.

63-76. (canceled)

77. (currently amended) The microprocessor system of claim 45, wherein:
at least said MPU, said IOP, and said MIF are located on-chip; and
said CMOS oscillator is located ~~off-chip~~ off-chip.

78. (previously presented) The microprocessor system of claim 77, wherein:
said clock multiplier is located on-chip.

79. (previously presented) The microprocessor system of claim 77, wherein:
said clock multiplier includes at least one phase locked loop circuit.

80. (previously presented) The microprocessor system of claim 77, wherein:
a frequency of said oscillator is quadrupled internally; and
said quadrupled frequency is used by said MIF.

81. (previously presented) The microprocessor system of claim 45, wherein:
said MPU is operative to execute a first instruction stream; and
said IOP is operative to execute a second instruction stream different than said first instruction stream executed by said MPU.

82. (previously presented) The microprocessor system of claim 81, wherein:
said IOP executes said second instruction stream to cause data to be transferred.

83. (previously presented) The microprocessor system of claim 45, further comprising:
a bus utilized by at least said MPU and said IOP; and wherein
said MIF is operative to arbitrate and prioritize a plurality of bus transaction requests generated by said MPU and said IOP, said bus transaction requests associated with said bus.

84. (currently amended) The microprocessor system of ~~claim 82~~ claim 83, wherein:
said MIF gives priority to said bus transaction requests generated by said IOP over said bus transaction requests generated by said MPU.

85. (currently amended) The microprocessor system of ~~claim 82~~ claim 83, wherein:
said bus is further utilized by said DMAC; and
said MIF is further operative to arbitrate and prioritize said bus transaction requests generated by said MPU, said IOP, and said DMAC.